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UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No. NEC00P267-hk
Total Pages in this Submission

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

and invented by:

1) **Ken Inoue**
2) **Masayuki Hamada**

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below

2. ☒ Specification having 19 pages and including the following:

   a. ☒ Descriptive Title of the Invention

   b. ☐ Cross References to Related Applications *(if applicable)*

   c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*

   d. ☐ Reference to Microfiche Appendix *(if applicable)*

   e. ☒ Background of the Invention

   f. ☒ Brief Summary of the Invention

   g. ☒ Brief Description of the Drawings *(if drawings filed)*

   h. ☒ Detailed Description

   i. ☒ Claim(s) as Classified Below

   j. ☒ Abstract of the Disclosure

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Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*

   a. ☒ Formal Number of Sheets **6 (Figs. 1-10)**

   b. ☐ Informal Number of Sheets _____

4. ☒ Oath or Declaration

   a. ☒ Newly executed *(original or copy)* ☐ Unexecuted

   b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*

   c. ☒ With Power of Attorney ☐ Without Power of Attorney

   d. ☐ *DELETION OF INVENTOR(S)*
   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).

5. ☐ Incorporation By Reference *(usable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ☐ Computer Program in Microfiche *(Appendix)*

7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*

   a. ☐ Paper Copy

   b. ☐ Computer Readable Copy *(identical to computer copy)*

   c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☒ Assignment Papers *(cover sheet & document(s))*

9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*

10. ☐ English Translation Document *(if applicable)*

11. ☒ Information Disclosure Statement/PTO-1449 ☒ Copies of IDS Citations

12. ☐ Preliminary Amendment

13. ☒ Acknowledgment postcard

14. ☐ Certificate of Mailing

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Accompanying Application Parts (Continued)

15. ☒ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Additional Enclosures *(please identify below):*

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	14	- 20 =	0	x	$18.00	$0.00
Indep. Claims	4	- 3 =	1	x	$78.00	$78.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$690.00
OTHER FEE *(specify purpose)*		Recordation of Assignment				$40.00
					TOTAL FILING FEE	$808.00

☒ A check in the amount of **$808.00** to cover the filing fee is enclosed.

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- ☐ Charge the amount of as filing fee.
- ☒ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Signature

Dated: **September 22, 2000**

Sean M. McGinn, Esq.
Registration No. 34,386

cc:

Customer No. 21254

P01ULRG/REV04

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APPLICATION FOR UNITED STATES LETTERS PATENT

APPLICANT: Ken Inoue
Masayuki Hamada

FOR: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

DOCKET NO.: NEC00P267-hk

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device and a manufacturing method thereof and more particularly to an improvement on a SOC (System On Chip) that has a logic (logic circuit) and a DRAM (Dynamic Random Access Memory) together on one and the same substrate.

2.Description of the Related Art

In a general purpose DRAM (having, on one chip, only a memory section and an adjacent circuit section which comprises a decoder, a sense amplifier, an I/O (input/output) circuit and the like), hold characteristics of memory cells have been, hitherto, regarded as the matter of great importance so that it has become a common practice to set the dopant concentration in the source-drain regions of cell transistors lower than that in the adjacent circuit section for the purpose of achieving the suppression of the junction leakage current.

Meanwhile, in recent years, demands that image processing using computer graphics should be made at a higher speed have been growing. Accordingly, there has been proposed a DRAM-incorporated logic chip as shown in Fig. 9, a so-called

SOC **31** which has a DRAM section **32** comprising memory cells **33** and adjacent circuits **34** such as a decoder and a sense amplifier, a logical operation section (a logic section) **35** where graphic processing is carried out at a high speed, and, in addition, an I/O section **36** which connects these DRAM and logic sections with an external circuit, all together on one chip.

In the DRAM section thereof, to suppress the short channel effect and relax the centralization of the drain field, the dopant concentration in the source-drain (S/D) should be, hitherto, set low. This makes the junction in the S/D regions shallow and, as has been pointed out, the silicidation therein may bring about an increase in the leakage current. In light of this problem, several techniques of making silicidation in the DRAM section have been proposed

For example, Japanese Patent Application Laid-open No. 97649/1999 discloses the methods using the following SOC structures: that is, (1) a structure (first embodiment) wherein, while the dopant concentration in S/D regions of a memory cell region in a DRAM section is set low to make the leakage small, dopants are implanted into S/D regions of an adjacent circuit region to a high concentration, and besides silicide layers are formed on gate surfaces and the surfaces of active regions, and thereby high-speed operations become

attainable; (2) a structure (second embodiment) wherein, in a DRAM cell section, S/D regions (low dopant-concentration regions) with which capacitor contacts are connected are set as non-silicide regions, and silicide layers are formed only on the surfaces of S/D regions (low dopant-concentration regions) with which bit line contacts are connected and on the gate surfaces of cell transistors, whereby the interconnection resistance and the contact resistance are reduced, and reading and writing operations at a higher speed are made attainable; and (3) a structure (third embodiment) wherein, in a DRAM memory cell section, portions of a TEOS (Tetra-Ethyl-Ortho-Silicate) oxide film that is first laid at the time of formation of transistor sidewalls are selectively left at the edge of LOCOS (Local Oxidation of Silicon), or in the vicinity of bird' s beaks, and thereafter silicide layers are formed on the entire surface of the DRAM memory cell section but said portions, in the same way as for cell gates and a logic section, and thereby reading and writing operations at a higher speed are made attainable, while the junction leakage is kept low. As an example, the third embodiment in said publication is now described in detail with reference to a schematic cross-sectional view of a memory cell section shown in Fig. 10. A semiconductor substrate **41** is isolated into elements by isolation oxide films **42** and a memory

cell transistor is formed between these films. Silicide layers **49** are formed on the surfaces of the gate electrodes **48** and in regions where a contact **52a** connecting with a bit line **51** and contacts **52b** connecting with storage nodes **53** are in contact with the semiconductor substrate **41**, respectively. These silicide layers lying on the substrate are formed within low dopant-concentration regions **47**. At the edge sections of the isolation oxide films **42**, there are formed TEOS oxide films **50**, protecting these edge sections from silicidation, so that silicide layers may not be formed beneath the isolation oxide films **42** or the junction leakage may not be generated around the edges thereof. In the drawing, **43-45** each represents an interlayer insulating film; **46**, gate oxide films; **54**, a dielectric film and **55**, a cell plate.

Further, Japanese Patent Application Laid-open No.17129/1999 discloses a structure wherein, after S/D regions of transistors in a DRAM cell section and a logic section are formed in separate steps, respectively, and contact-holes that reach S/D regions of transistors for cell selection are formed, silicide layers are formed on the surfaces of the S/D regions through said contact-holes so that conductive films are buried in the contact-holes. In this instance, silicide layers are also formed in the S/D regions of transistors in the logic section but this silicidation is

carried out in a different step from the one for silicidation of the S/D regions of transistors for cell selection. Further, it is therein mentioned that silicidation can be also applied to the gate surfaces in another step.

In any of these conventional techniques, the S/D regions of DRAM cell transistors are still formed to have a low dopant concentration, while the S/D regions of transistors in the logic section, a high dopant concentration. In other words, a SOC structure of this sort is designed under the concept that a high-speed logic is made incorporated into an existing DRAM. This assumes fabrication of the DRAM section and the logic section in separate steps and, thus, a reduction of the production cost cannot be much expected to happen. However, the SOC is, by nature, designed and manufactured for each system application. In comparison with the general purpose DRAM, a small quantity and a large diversity characterize its production, and, therefore, the cost reduction has a particular significance.

SUMMARY OF THE INVENTION

An object of the present invention is, therefore, with such a pre-concept relinquished, to provide a manufacturing method that can produce, with low cost, an SOC having necessary and sufficient characteristics in the DRAM section, while

attaining higher-speed performance of the whole elements therein, on the basis of a novel concept that a DRAM is made incorporated into a high-speed logic, and a structure of the SOC thereat.

Accordingly, the present invention relates to a DRAM-incorporated semiconductor device which has a DRAM section and a logic section being formed on one and the same substrate, wherein silicide layers are formed, at least, on all the surfaces of the source-drain regions and the gate surfaces of transistors in the DRAM section and the logic section. Further, the present invention relates to a method of manufacturing a DRAM-incorporated semiconductor device in which a DRAM section and a logic section are formed on a semiconductor substrate that is isolated into elements, wherein silicidation of all the surfaces of the source-drain regions and the gate surfaces that constitute transistors in the DRAM section and the logic section is carried out concurrently in one and the same step.

Further, the present invention relates to a semiconductor device having a memory cell section and an adjacent circuit section, wherein silicide layers are formed on all the surfaces of the source-drain regions and the gate surfaces of transistors in the memory cell section and the adjacent circuit section.

In the present invention, the source-drain regions in the DRAM section are made high dopant-concentration regions and consequently, through silicidation of all the surfaces of said regions and the gate surfaces, good ohmic contacts can be formed. Further, the formation of silicide can be carried out concurrently with silicidation in the logic section in one and the same step. Therefore, an increase in the number of the steps in a manufacturing method can be avoided, and both higher-speed performance of the whole elements and lower cost production can be realized.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1-8 are a series of schematic cross-sectional views illustrating the steps of a manufacturing method of a semiconductor device that is one embodiment of the present invention.

Fig. 9 is a schematic view showing an example of the structure of a SOC having a DRAM on board.

Fig. 10 is a cross-sectional view showing a conventional DRAM cell section.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to the drawings, the present invention is described in detail below. Figs. 1-8 are a series of schematic

cross-sectional views illustrating the steps of a manufacturing method of a semiconductor device that is one embodiment of the present invention.

First, onto a Si substrate **1**, buried oxide films **2** are formed by the known method of trench isolation so as to isolate an N-MOS (N-Metal-Oxide-Semiconductor) and a P-MOS of a logic section and a DRAM section each as an element. Next, over the surface of the substrate **1**, a thin oxide film (a SiO_2: sacrifice oxide film, not shown in the drawing) is formed by thermal oxidation, and then the channel ion implantation for forming P-channels and N-channels to the logic section and adjacent circuits which comprise a decoder and a sense amplifier in the DRAM section, an I/O circuit and the like, and forming N-channels to memory cells, together with the ion implantation for forming respective wells (a P-well **3**, an N-well **4** and a cell P-well **5**) are performed. This accomplishes formation of the structure shown in Fig.1. Although Fig. 1 shows, for the sake of simplification, only respective wells, buried oxide films **2** for element isolation and a memory cell in the DRAM section, it is apparent that the present invention is not limited to this structure. Further, the ion implantation for the cell P-well **5** and the P-well **3** may be performed simultaneously or separately. A deep N-well may be additionally formed in the memory cell region.

After removing the sacrifice oxide film, a gate oxide film (not shown in the drawing) is formed by another thermal oxidation. Hereat, it is preferable to make the gate oxide film thicker in the DRAM section than in the logic section. A polysilicon layer that is to serve as respective gates of all transistors is, then, formed over the entire surface and patterned into a prescribed shape of gate electrodes. After that, dopant ions are implanted thereinto so as to form LDD (Lightly-Doped Drain) regions **7a**, **7b** and **7c**, in respective sections. Formation of the LDD regions **7a** and **7c** may be performed, hereat, simultaneously or separately.

Subsequently, using TEOS or the like, an oxide film is grown over the entire surface by the CVD (Chemical Vapour Deposition) method and, through anisotropic etching, LDD sidewalls **8** are formed on lateral faces of gate electrodes (Fig. 2).

Next, as shown in Fig. 3, masking the N-MOS section and the DRAM section with a resist **9a**, only the P-MOS section is left exposed, and p-type dopants such as B or BF_2 are ion-implanted for formation of the S/D regions **10a** in the P-MOS section. For example, BF_2 is ion-implanted under the conditions that the accelerating voltage is 20 keV and the dose is 3E15 or so. Hereat, the gate polysilicon is also subjected to the ion implantation simultaneously and, as a result, becomes a P-gate.

Next, as shown in Fig. 4, a resist **9b** is formed only in the P-MOS section, and n-type dopants such as P or As are ion-implanted into the N-MOS section and the DRAM section, for example, As is ion-implanted at 50 keV to a dose of 3E15-6E15 or so, thus forming S/D regions **10b** and **10c**, respectively. Hereat, the gate polysilicons are also subjected to the ion implantation simultaneously and, as a result, become N-gates. In effect, there are formed so-called P-N gates in which the P-ch has a P-gate and the N-ch , an N-gate. After that, for example, the RTA (Rapid Thermal Annealing) (ramp annealing) is performed at 1000 °C for 10 seconds or so, and the implanted dopants are activated. While ion-implantation is, hereat, applied to the N-MOS section and the DRAM section at the same time, it can be applied to each in separate steps.

Next, as shown in Fig. 5, a metal film for silicidation is grown over the entire surface by the sputtering method or the like. Here, an example in which a cobalt (Co) film **11** is grown is shown. However, the present invention is not limited to this and any metal material that can form silicide through a thermal reaction with silicon, such as titanium and nickel, can be utilized in the same manner.

Next, the unreacted Co film **11** is removed by a heat treatment. For example, a heat treatment in N_2 gas atmosphere at a temperature of 500-600 °C or so is applied thereto for

30 seconds and then the unreacted Co film is removed with a mixed solution of sulfuric acid and hydrogen peroxide, and another heat treatment in the nitrogen gas atmosphere at 800 °C is further applied thereto for 10 seconds or so (the so-called salicide method), which results in formation of cobalt silicide ($CoSi_2$) **12** over all the surfaces of the S/D regions (**10**) and on the gate electrodes (**6**), as shown in Fig. 6.

Subsequently, in the same way as the prior art, a first interlayer film **13** is formed and thereafter contact holes to connect to capacitor electrodes are formed in the DRAM section, and then, by filling up the contact holes with a metal or a polysilicon, capacitor contacts **14** are formed. Lower electrodes **15**, capacitor insulating films which are omitted from the drawing and upper electrodes **16** are then formed to accomplish capacitor electrodes (Fig. 7). Although stacked-type capacitor electrodes are, herein, shown as lower electrodes, the present invention is, in no way, limited by this, and can have known cylindrical electrodes or electrodes with an even more complicated structure for them. When utilizing polysilicon, HSG (Hemispherical Silicon Grain) electrodes can be also employed. Further, the capacitor contacts, lower electrodes and upper electrodes may be formed, using a known material such as Ti/TiN/W or the like. In short,

the material, the structure and such can be selected appropriately for them according to design.

Following this, as shown in Fig. 8, after a second interlayer film **17** is formed, contacts **18** each connecting with one region of the S/D regions of transistors in the logic section and a bit line contact **19** connecting with the DRAM section are formed, using a known metal material such as Ti/TiN/W or the like. Next, a known interconnection material such as Al, TiN, W or the like is grown over the entire surface by the sputtering method and then patterned, whereby a first interconnection **20** that is also to serve as a bit line is formed. Obviously, the bit line and the first interconnection can be formed as different layers or from different materials.

Further, when forming contact holes, it is preferable to form an etching stopper layer on the substrate so that the pre-formed silicide layers may not be carved into at the time of etching.

What distinguishes the present invention from the conventional techniques the most is the fact that, even in the memory cell region of the DRAM section, there are formed the S/D regions with a high dopant concentration defined as n^+. When silicide is formed on the S/D regions with such a high dopant concentration, good ohmic contacts can be formed. Further, because the junction becomes deeper, the junction

leakage current is hardly generated even if silicide is formed over all the surfaces of the S/D regions. In contrast with this, when silicide is formed on conventional low dopant-concentration regions (n^-), Schottkey contacts are formed therebetween, which is not adequate for the purpose of achieving lower resistance.

Further, by setting the S/D regions of the memory cell regions as high dopant-concentration regions, good ohmic contacts can be formed through silicidation, as described above, so that this invention can be readily put into practice. Moreover, as the present invention has a considerable effect of making the performance of the whole elements faster and the steps of a manufacturing method simpler, its technical significance cannot be overemphasized.

While, for the above description, a DRAM-incorporated SOC is given as an example, the present invention can be applied to a semiconductor device that does not have any logic section, that is, a semiconductor device having only a DRAM section. Further, the present invention can be applied to a semiconductor device having a DRAM cell section and an adjacent-circuit-functional element section, wherein silicide layers are formed over all the surfaces of the source-drain regions and the gate surfaces of transistors in the DRAM cell section and the adjacent-circuit-functional

element section which comprises elements such as various decoders, sense amplifiers and the like. In this instance, too, silicidation of the DRAM cell section and the adjacent circuit section can be carried out concurrently in one and the same step, in accordance with the above description, and thereby both higher-speed performance of the whole elements and simplification of the manufacturing steps can be attained.

WHAT IS CLAIMED IS:

1. A DRAM-incorporated semiconductor device which has a DRAM section and a logic section being formed on one and the same substrate, wherein silicide layers are formed, at least, on all the surfaces of the source-drain regions and the gate surfaces of transistors in the DRAM section and the logic section.

2. The semiconductor device according to Claim 1, wherein said silicide is selected from the group consisting of titanium silicide, cobalt silicide and nickel silicide.

3. The semiconductor device according to Claim 1, wherein gates of transistors in said DRAM section and logic section are all P-N gates.

4. The semiconductor device according to Claim 1, which has a bit contact connecting the DRAM section with a bit line and a contact plug connecting to the source-drain in the logic section, with each of these contacts being formed of a metal material.

5. A method of manufacturing a DRAM-incorporated semiconductor device in which a DRAM section and a logic section are formed on a semiconductor substrate that is isolated into elements, wherein silicidation of all the surfaces of the source-drain regions and the gate surfaces that constitute transistors in the DRAM section and the logic section is carried out concurrently in one and the same step.

6. The method of manufacturing a semiconductor device according to Claim 5, wherein said step of silicidation comprises forming a metal film over the entire surface of the substrate, and thereafter performing a heat treatment to remove the unreacted metal film.

7. The method of manufacturing a semiconductor device according to Claim 6, wherein said metal film is selected from the group consisting of titanium, cobalt and nickel.

8. The method of manufacturing a semiconductor device according to Claim 5, wherein dopant implantation into gates are carried out concurrently with formation of the source-drain regions that constitute transistors in the DRAM section and the logic section, and thereby P-N gates are formed.

9. The method of manufacturing a semiconductor device according to Claim 5, which further comprises the step of forming a bit contact connecting the DRAM section with a bit line and a contact plug connecting to the source-drain in the logic section, with each of these contacts being formed of a metal material.

10. A semiconductor device having a memory cell section and an adjacent circuit section, wherein silicide layers are formed on all the surfaces of the source-drain regions and the gate surfaces of transistors in the memory cell section and the adjacent circuit section.

11. The semiconductor device according to Claim 10, wherein said silicide is selected from the group consisting of titanium silicide, cobalt silicide and nickel silicide.

12. A method of manufacturing a semiconductor device having a memory cell section and an adjacent circuit section, wherein silicidation of all the surfaces of the source-drain regions and the gate surfaces of transistors in the memory cell section and the adjacent circuit section is carried out concurrently in one and the same step.

13. The method of manufacturing a semiconductor device according to Claim 12, wherein said step of silicidation comprises forming a metal film over the entire surface of the substrate, and thereafter performing a heat treatment to remove the unreacted metal film.

14. The method of manufacturing a semiconductor device according to Claim 13, wherein said metal film is selected from the group consisting of titanium, cobalt and nickel.

ABSTRACT OF THE DISCLOSURE

In a DRAM-incorporated semiconductor device (SOC) which has a DRAM section and a logic section being formed on one and the same substrate, with the object of providing, with low cost, a SOC having necessary and sufficient characteristics in the DRAM section, while attaining higher-speed performance of the whole elements, silicide is formed at least on all the surfaces of the source-drain regions (**10**) and the gate surfaces (**6**) of transistors in the DRAM section and the logic section, concurrently in one and the same step.

FIG.1

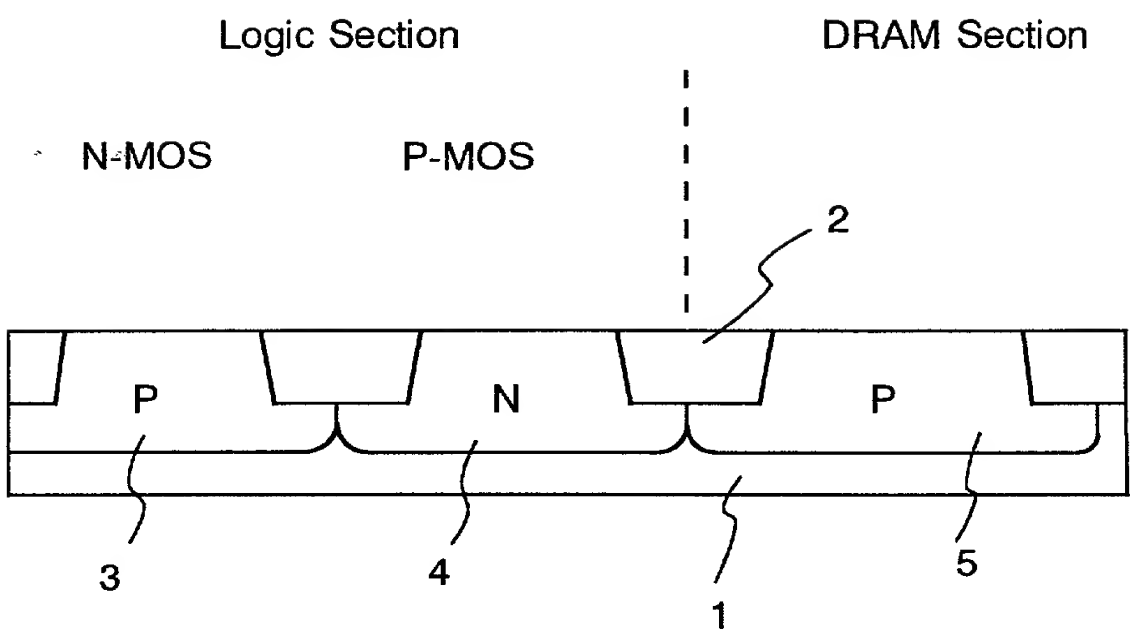

Logic Section
DRAM Section
N-MOS
P-MOS
2
P
N
P
3
4
1
5

FIG.2

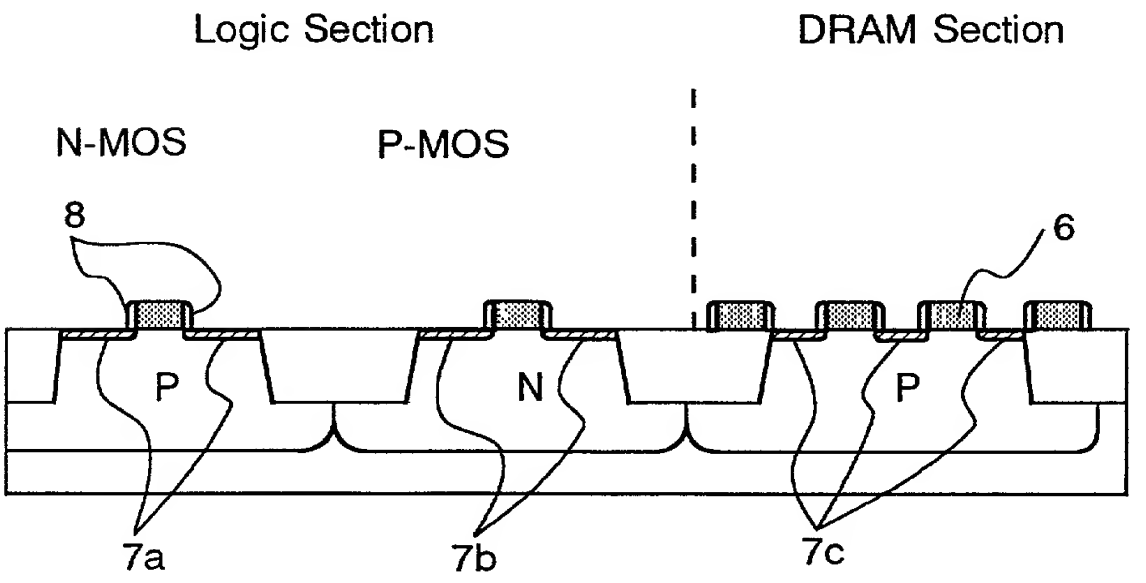

Logic Section
DRAM Section
N-MOS
P-MOS
8
6
P
N
P
7a
7b
7c

FIG.3

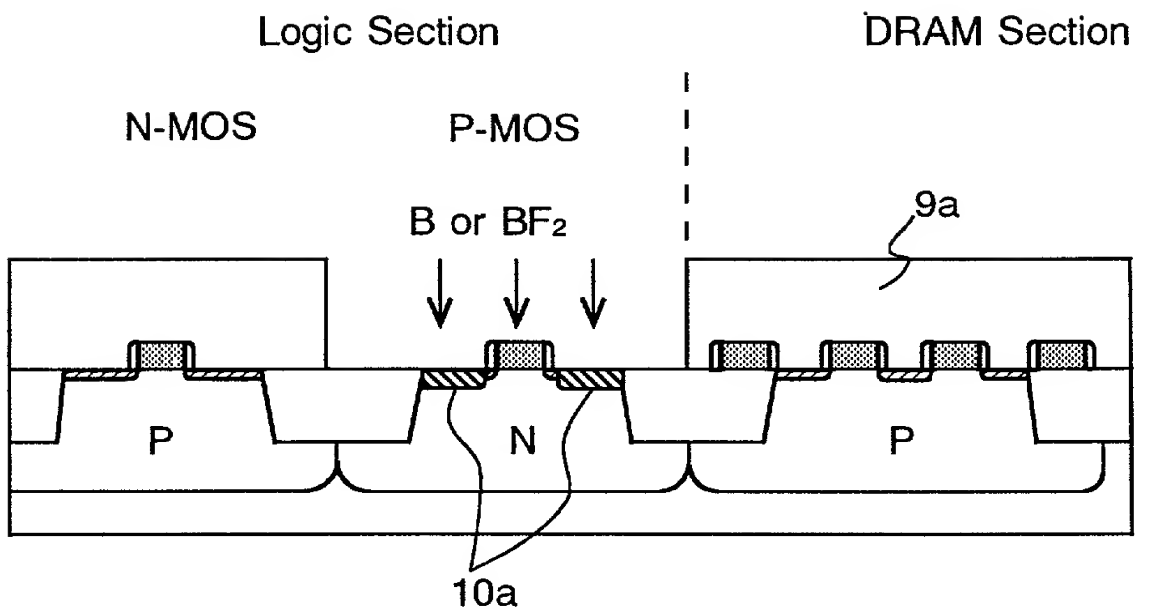

Logic Section
DRAM Section
N-MOS
P-MOS
B or BF2
9a
P
N
P
10a

FIG.4

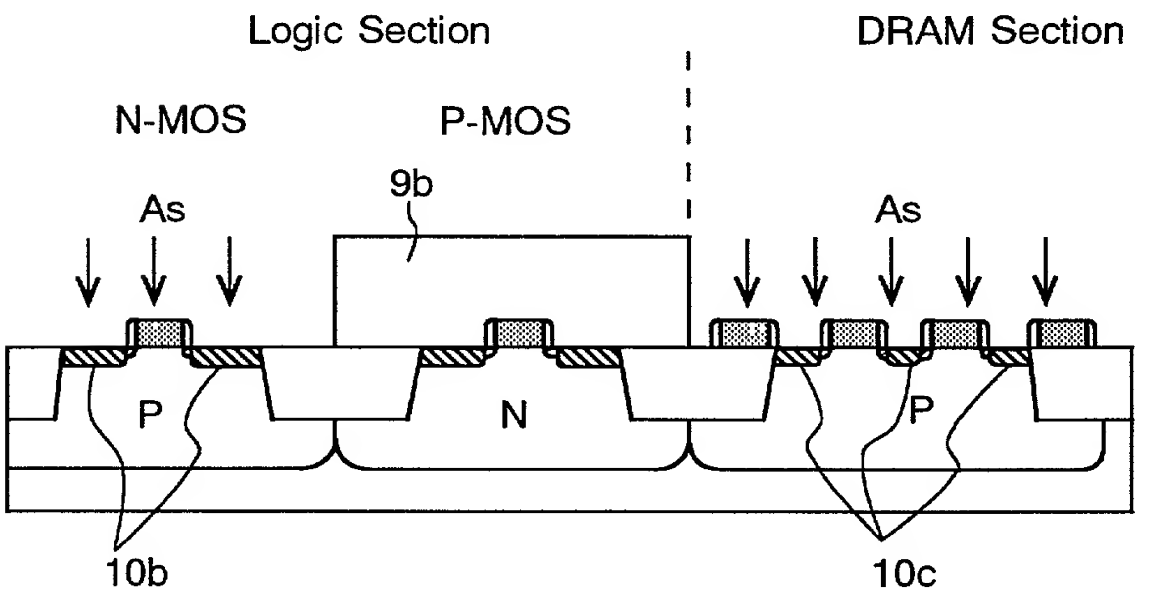

Logic Section
DRAM Section
N-MOS
P-MOS
9b
As
As
P
N
P
10b
10c

FIG.5

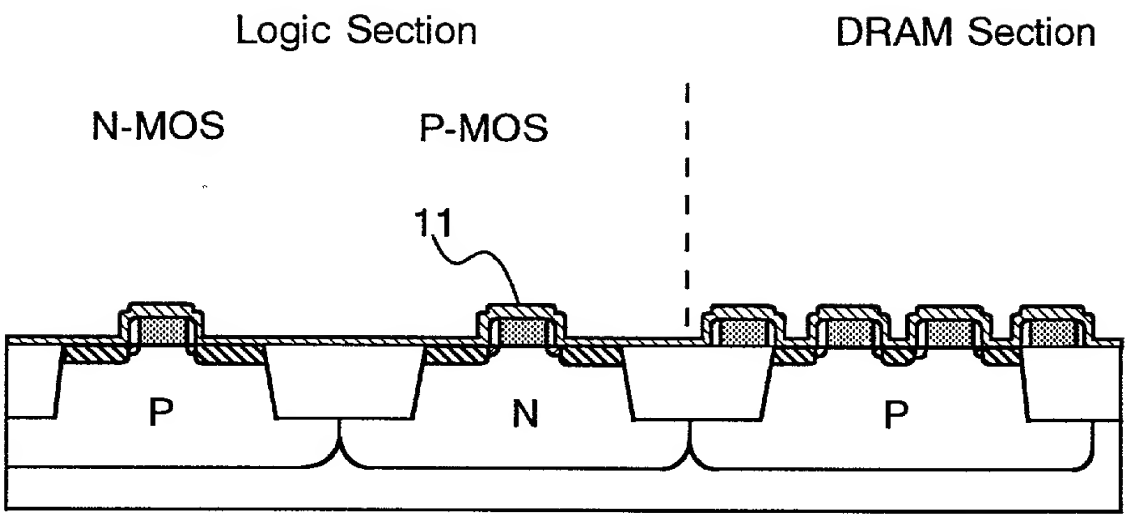

Logic Section
DRAM Section
N-MOS
P-MOS
11
P
N
P

FIG.6

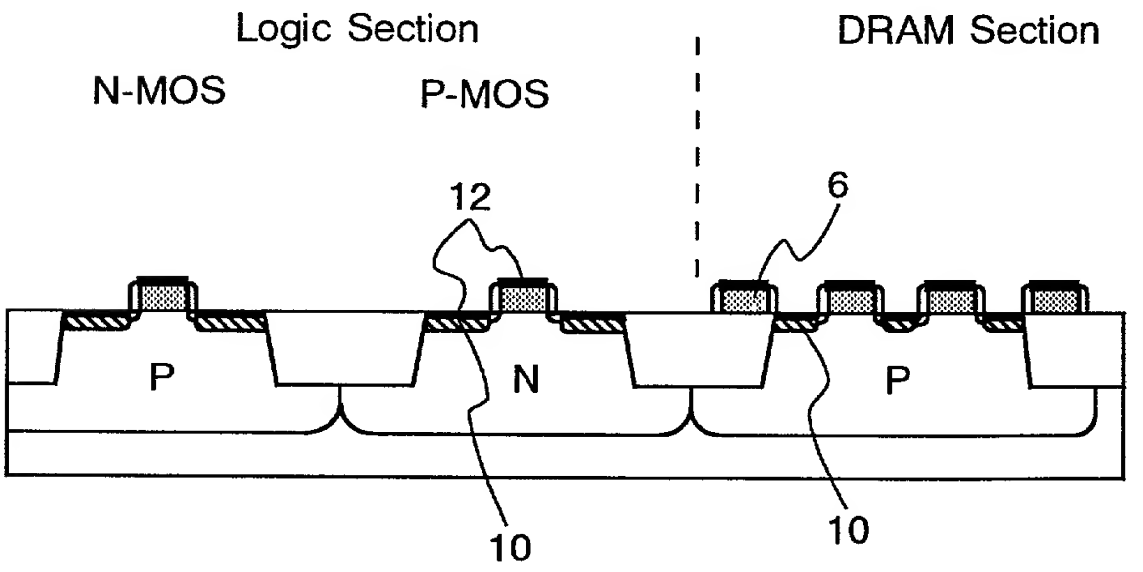

Logic Section
DRAM Section
N-MOS
P-MOS
12
6
P
N
P
10
10

FIG.7

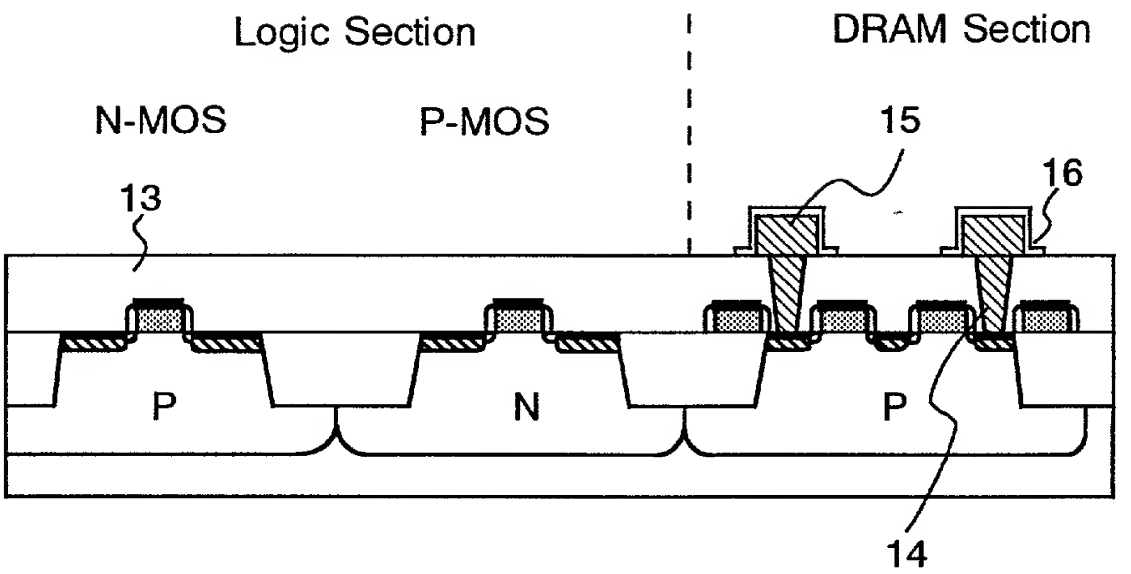

Logic Section
DRAM Section
N-MOS
P-MOS
15
16
13
P
N
P
14

FIG.8

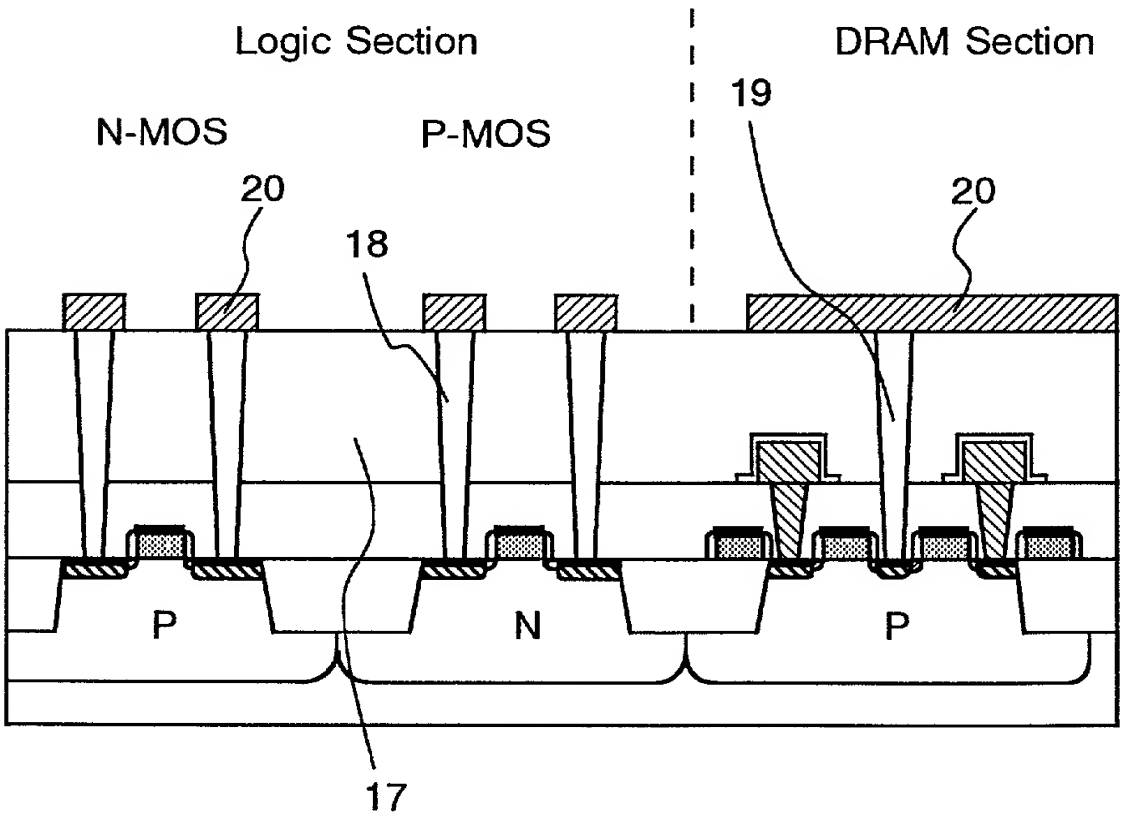

Logic Section
DRAM Section
19
N-MOS
P-MOS
20
18
20
P
N
P
17

FIG.9
(Prior Art)

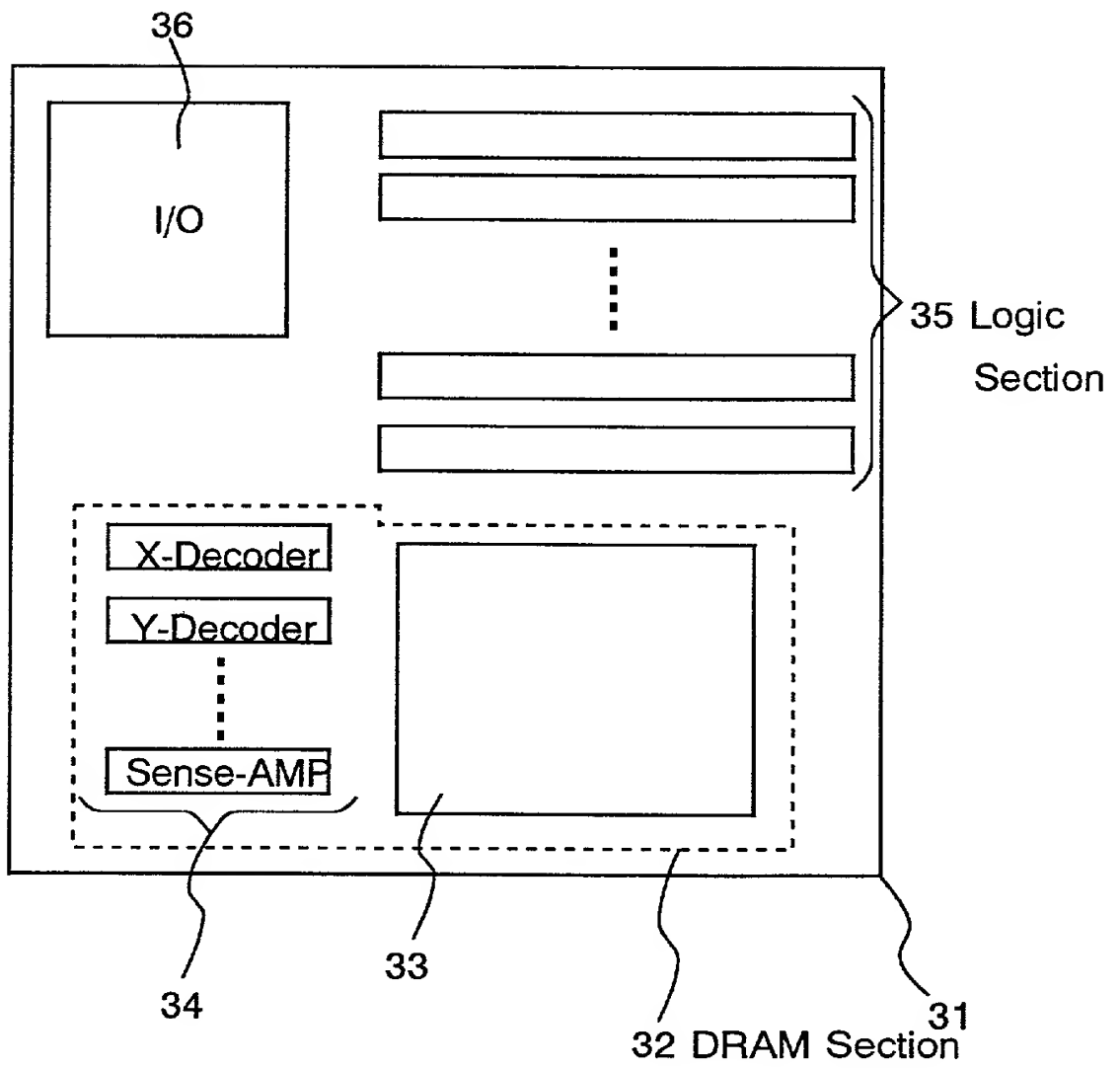
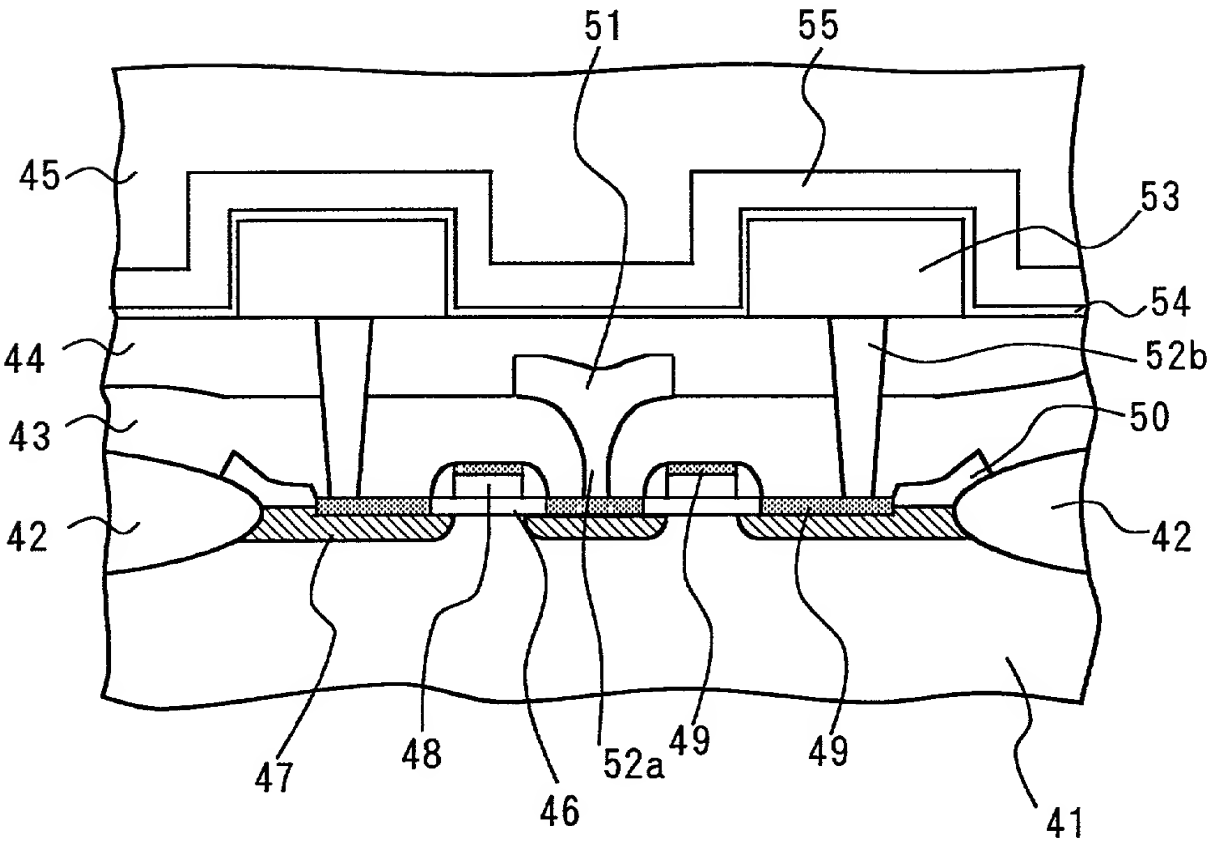


FIG.10
(Prior Art)



Application for United States Patent

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

the specification of which:
(check one)

X (is attached hereto)
___ was filed on _____,
as Application Serial No. _____
and was amended on _____. (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56*

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			**priority claimed**	
305702/1999	Japan	27/10/1999	X	
(Number)	(Country)	(Day/Month/Year Filed)	yes	no
(Number)	(Country)	(Day/Month/Year Filed)	yes	no
(Number)	(Country)	(Day/Month/Year Filed)	yes	no

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)

Power of Attorney: As a named inventor, I hereby appoint Sean M. McGinn, Reg. No. 34, 386, and Frederick W. Gibb, III, Reg. No. 37,629, as attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. All correspondence should be directed to **McGinn & Gibb, P.C., 1701 Clarendon Boulevard, Suite 100, Arlington, Virginia 22209**. Telephone calls should be directed to McGinn & Gibb, P.C. at (703) 294-6699.

I hereby declare that all statements made herein of my own knowledge are true arid that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole
or First Inventor Ken INOUE

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Full Name of Third
Joint Inventor, If Any _____

Inventor's Signature _____ Date _____

Residence _____

Citizenship _____

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Full Name of Fourth
Joint Inventor, If Any _____

Inventor's Signature _____ Date _____

Residence _____

Citizenship _____

Post Office Address _____

(An additional sheet(s) is/are attached hereto if the present invention includes more than four inventors.)

*Title 37, Code of Federal Regulations, § 1.56:

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith toward the Patent and Trademark Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and (1) it establishes by itself or in combination with other information, a prima facie case of unpatentability; or (2) it refutes, or is inconsistent with, a position the applicant takes in: (i) opposing an argument of unpatentability relied on by the Office, or (ii) asserting an argument of patentability.